What is claimed is:

1.   A semiconductor circuit designing apparatus, comprising:

a circuit design unit executing a logical design of a semiconductor integrated circuit; and

5   an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to an inspection item of a inspection to be executed before a layout design of said semiconductor integrated

10 circuit is executed, and

wherein said circuit design unit generates a target circuit feature information indicating said circuit feature of a target semiconductor integrated circuit of said semiconductor

15 integrated circuit of which said logical design should be executed, and

wherein said circuit design unit obtains a target inspection item of said inspection item corresponding to said target circuit feature

20 information from said inspection item database section, and

wherein said circuit design unit executes said logical design of said target semiconductor integrated circuit in reference to said target

25 inspection item.

2.   The semiconductor circuit designing
apparatus according to Claim 1, further
comprising:

        a model development history database
5   section in which an ID data of said circuit design
unit corresponds to the number of times said
circuit design unit failed said inspection of said
inspection item previously, and

        wherein said target inspection item is
10 determined such that said inspection item of which
said number of times is smaller than a
predetermined value is withdrawn from said target
inspection item.

3.   The semiconductor circuit designing
apparatus according to Claim 1, further
comprising:

        a layout design unit executing said layout
5   design, and

        wherein said circuit design unit executes
said inspection of said target semiconductor
integrated circuit of which said layout design is
executed, with regard to said target inspection
10 item, and

        wherein said circuit design unit provides a
result of said inspection with said target
semiconductor integrated circuit to said layout

design unit.

4.   The semiconductor circuit designing
apparatus according to Claim 2, further
comprising:
      a layout design unit executing said layout
5   design, and
      wherein said circuit design unit executes
said inspection of said target semiconductor
integrated circuit of which said layout design is
executed, with regard to said target inspection
10   item, and
      wherein said circuit design unit provides a
result of said inspection with said target
semiconductor integrated circuit to said layout
design unit.

5.   The semiconductor circuit designing
apparatus according to Claim 4, wherein when said
provided result of said inspection has no problem,
said layout design unit stores said ID data of
5   said circuit design unit and said number of times
said circuit design unit failed said inspection of
said target inspection item in said model
development history database section.

6.   The semiconductor circuit designing

apparatus according to Claim 1, wherein said inspection item database section belongs to said circuit design unit.

7.   The semiconductor circuit designing apparatus according to Claim 2, wherein said inspection item database section belongs to said circuit design unit.

8.   The semiconductor circuit designing apparatus according to Claim 3, wherein said inspection item database section belongs to said layout design unit.

9.   The semiconductor circuit designing apparatus according to Claim 4, wherein said inspection item database section belongs to said layout design unit.

10.   The semiconductor circuit designing apparatus according to Claim 5, wherein said inspection item database section belongs to said layout design unit.

11.   The semiconductor circuit designing apparatus according to Claim 3, wherein said layout design unit includes a plurality of layout

design sections, and

5   wherein said inspection item database

section belongs to at least one of said plurality

of layout design sections.

12.   The semiconductor circuit designing

apparatus according to Claim 3, further

comprising:

      a data center provided to be different from

5 said circuit design unit and said layout design

unit, and

      wherein said inspection item database

section belongs to said data center.

13.   A semiconductor circuit designing method,

comprising:

      (a) providing a inspection item database

section in which a circuit feature of a

5 semiconductor integrated circuit in which a

logical design should be executed corresponds to

an inspection item of a inspection to be executed

before a layout design of said semiconductor

integrated circuit is executed;

10   (b) notifying a circuit designer executing

said logical design of said semiconductor

integrated circuit of said inspection item

corresponding to said semiconductor integrated

circuit retrieved from said inspection item

15   database section; and

        (c) executing said logical design of said
semiconductor integrated circuit by said circuit
designer in reference to said notified inspection
item.

14.   The semiconductor circuit designing method
according to Claim 13, further comprising:
        (d) providing said semiconductor integrated
circuit in which said notified inspection item is
5   passed to a layout designer executing said layout
design.

15.   The semiconductor circuit designing method,
comprising:
        (e) providing a circuit design unit
executing a logical design of a semiconductor
5   integrated circuit; and
        (f) providing an inspection item database
section in which a circuit feature of said
semiconductor integrated circuit corresponds to an
inspection item of a inspection to be executed
10   before a layout design of said semiconductor
integrated circuit is executed, and
        wherein said circuit design unit generates
a target circuit feature information indicating

said circuit feature of a target semiconductor

15   integrated circuit of said semiconductor

integrated circuit of which said logical design

should be executed, and

wherein said circuit design unit obtains a

target inspection item of said inspection item

20   corresponding to said target circuit feature

information from said inspection item database

section, and

wherein said circuit design unit executes

said logical design of said target semiconductor

25   integrated circuit in reference to said target

inspection item.

16.   The semiconductor circuit designing method

according to Claim 15, further comprising:

(g) providing a model development history

database section in which an ID data of said

5   circuit design unit corresponds to the number of

times said circuit design unit failed said

inspection of said inspection item previously, and

wherein said target inspection item is

determined such that said inspection item of which

10   said number of times is smaller than a

predetermined value is withdrawn from said target

inspection item.

17.   The semiconductor circuit designing method
according to Claim 15, further comprising:

(h) providing a layout design unit
executing said layout design, and

5   wherein said circuit design unit executes
said inspection of said target semiconductor
integrated circuit of which said layout design is
executed, with regard to said target inspection
item, and

10   wherein said circuit design unit provides a
result of said inspection with said target
semiconductor integrated circuit to said layout
design unit.

18.   The semiconductor circuit designing method
according to Claim 16, further comprising:

(i) providing a layout design unit
executing said layout design, and

5   wherein said circuit design unit executes
said inspection of said target semiconductor
integrated circuit of which said layout design is
executed, with regard to said target inspection
item, and

10   wherein said circuit design unit provides a
result of said inspection with said target
semiconductor integrated circuit to said layout
design unit.

19.   The semiconductor circuit designing method
according to Claim 18, wherein when said provided
result of said inspection has no problem, said
layout design unit stores said ID data of said
5 circuit design unit and said number of times said
circuit design unit failed said inspection of said
target inspection item in said model development
history database section.

20.   The semiconductor circuit designing method
according to Claim 15, wherein said inspection
item database section belongs to said circuit
design unit.